Amendments to the Claims:

1. (original) A computer system comprising:

a host entity for issuing IO requests;

an external JBOD emulation controller coupled to the host entity for emulating IO operations in response to the IO requests; and

a set of at least one physical storage device coupled to the JBOD emulation controller each through a point-to-point serial-signal interconnect for providing storage to the computer system through the JBOD emulation controller, wherein

said JBOD emulation controller is capable of defining at least one logical media unit (LMU) comprising sections of at least one of the physical storage devices and bringing the LMU on line or taking the LMU off line while the JBOD emulation controller is on line.

2. (original) The computer system of claim 1 wherein the point-to-point serial-signal interconnect is a Serial ATA IO device interconnect.

3. (original) The computer system of claim 1 wherein the point-to-point serial-signal interconnect is a Serial-Attached SCSI (SAS) IO device interconnect.

4. (original) The computer system of one of claims 1 through 3 wherein said external JBOD emulation controller comprises

a central processing circuitry for performing IO operations in response to said IO requests of said host entity;

at least one IO device interconnect controller coupled to said central processing circuitry;

at least one host-side IO device interconnect port provided in a said at least one IO device interconnect controller for coupling to said host entity; and

at least one device-side IO device interconnect port provided in a said at least one IO device interconnect controller for coupling to a said at least one physical storage device.

5. (original) The computer system of claim 4 wherein said LMU are presented redundantly to the host entity on more than one host-side IO device interconnect port.

6. (original) The computer system of one of claims 1 through 3, further comprises a second external JBOD emulation controller coupled to the host entity for emulating IO operations in response to the IO requests, wherein said external JBOD emulation controller and said second external JBOD emulation controller are configured into a redundant pair, and said LMU is allowed to be brought on line or taken off line while the JBOD emulation controller is on line.

7. (original) The computer system of claim 6, wherein said LMU can be redundantly presented to the host by both of said external JBOD emulation controllers.

8. (original) A JBOD subsystem for providing storage to a host entity, comprising:
at least one external JBOD emulation controller for coupling to the host entity for emulating IO operations in response to IO requests issued from the host entity; and
a set of at least one physical storage device each coupled to the JBOD emulation controller through a point-to-point serial-signal interconnect for providing storage to the host entity through the JBOD emulation controller, wherein
said JBOD emulation controller is capable of defining at least one logical media unit (LMU) comprising sections of at least one of the physical storage devices and bringing a said LMU on line or taking a said LMU off line while the JBOD emulation controller is on line.

9. (original) The JBOD subsystem of claim 8 wherein the point-to-point serial-signal interconnect is a Serial ATA IO device interconnect.

10. (original) The JBOD subsystem of claim 8 wherein the point-to-point serial-signal interconnect is a Serial-Attached SCSI (SAS) IO device interconnect.

11. (original) The JBOD subsystem of one of claims 8 through 10 wherein a said at least one LMU comprises sections of a plurality of the physical storage devices.

12. (original) The JBOD subsystem of one of claims 8 through 10 wherein said external JBOD emulation controller comprises

a central processing circuitry for performing IO operations in response to said IO requests of said host entity;

at least one IO device interconnect controller coupled to said central processing circuitry;

at least one host-side IO device interconnect port provided in a said at least one IO device interconnect controller for coupling to said host entity; and

at least one device-side IO device interconnect port provided in a said at least one IO device interconnect controller for coupling to a said at least one physical storage device.

13. (original) The JBOD subsystem of one of claims 8 through 10, further comprising auto-on-lining mechanism to automatically bring on line a said LMU which was previously off-line once a requisite quorum of said PSDs comes on-line.

14. (original) The JBOD subsystem of one of claims 8 through 10, further comprising auto-off-lining mechanism to automatically take off line a said LMU which was

previously on-line once a requisite quorum of said PSDs becomes off-line.

15. (original) The JBOD subsystem of one of claims 8 through 10, further comprising determining mechanism for automatically determining when a PSD has been removed or when one has been inserted.

16. (original) The JBOD subsystem of one of claims 8 through 10, further comprising scanning-in mechanism to automatically scan in PSDs on detection of insertion of the PSD.

17. (original) The JBOD subsystem of one of claims 8 through 10, further comprising informing mechanism for informing the host entity when the mapping of said LMUs to host-side interconnect LUNs has changed.

18. (original) The JBOD subsystem of one of claims 8 through 10, further comprising unique ID determination mechanism to uniquely identify said PSDs independent of their location in which they are installed in the JBOD subsystem.

19. (original) The JBOD subsystem of claim 18, wherein information used to uniquely identify each of said PSDs is stored on the PSD.

20. (original) The JBOD subsystem of one of claims 8 through 10, wherein LMU identification and configuration information is stored on the member PSDs that compose the LMU.

21. (original) The JBOD subsystem of claim 20, wherein LMU identification information presented to the host entity is generated from said LMU identification information stored on the member PSDs that compose the LMU.

22. (original) The JBOD subsystem of one of claims 8 through 10, wherein LMU identification information presented to the host entity is generated from information stored in a non-volatile memory in the JBOD emulation controller.

23. (original) The JBOD subsystem of one of claims 8 through 10, wherein LMU identification information presented to the host entity is generated as follows: from information stored in a non-volatile memory in the JBOD subsystem prior to being able to obtain LMU identification information off of the member PSDs and from LMU identification information stored on the member PSDs that compose the LMU after the member PSDs become accessible.

24. (original) The JBOD subsystem of one of claims 8 through 10, wherein a first and a second of said at least one JBOD emulation controller are configured into a redundant pair, whereby when the first JBOD emulation controller goes off line or is taken off line, the second JBOD emulation controller will take over the functionality of the first JBOD emulation controller.

25. (original) The JBOD subsystem of claim 24, wherein a host-side port of said first JBOD emulation controller and a host-side port of said second JBOD emulation controller are configured into a complementary port pair.

26. (original) The JBOD subsystem of claim 25, wherein said complementary port pair are interconnected onto a same host-side IO device interconnect.

27. (original) The JBOD subsystem of claim 26, wherein said complementary port pair are interconnected together with switch circuitry.

28. (original) The JBOD subsystem of claim 25, wherein each port of said complementary port pair is interconnected onto a different host-side IO device interconnect.

29. (original) The JBOD subsystem of claim 24, wherein a said LMU is presented to the host entity through both said first and said second JBOD emulation controllers.

30. (original) The JBOD subsystem of one of claims 8 through 10, further comprising ID generation mechanism to automatically generate the LMU identification information presented to the host entity when a need arises.

31. (original) The JBOD subsystem of one of claims 8 through 10 wherein said LMU are presented redundantly to the host entity on more than one host-side IO device interconnect port.

32. (original) The JBOD subsystem of one of claims 8 through 10, further comprising an enclosure management services (EMS) mechanism.

33. (original) The JBOD subsystem of claim 32, wherein said EMS mechanism is of a direct-connect EMS configuration.

34. (original) The JBOD subsystem of claim 32, wherein said EMS mechanism is of a device-forward EMS configuration.

35. (original) The JBOD subsystem of claim 32, wherein said EMS mechanism implements both direct-connect and device-forward EMS configurations.

36. (original) The JBOD subsystem of claim 32, wherein said JBOD emulation controller is configured to support SES enclosure management services protocol.

37. (original) The JBOD subsystem of claim 32, wherein said JBOD emulation controller is configured to support SAF-TE enclosure management services protocol.

38. (original) The JBOD subsystem of one of claims 8 through 10, wherein at least one said host-side IO device interconnect port is Fibre Channel supporting point-to-point connectivity in target mode.

39. (original) The JBOD subsystem of one of claims 8 through 10, wherein at least one said host-side IO device interconnect port is Fibre Channel supporting public loop connectivity in target mode.

40. (original) The JBOD subsystem of one of claims 8 through 10, wherein at least one said host-side IO device interconnect port is Fibre Channel supporting private loop connectivity in target mode.

41. (original) The JBOD subsystem of one of claims 8 through 10, wherein at least one said host-side IO device interconnect port is parallel SCSI operating in target mode.

42. (original) The JBOD subsystem of one of claims 8 through 10, wherein at least one said host-side IO device interconnect port is ethernet supporting the iSCSI protocol operating in target mode.

43. (original) The JBOD subsystem of one of claims 8 through 10, wherein at least one said host-side IO device interconnect port is Serial-Attached SCSI (SAS) operating in target mode.

44. (original) The JBOD subsystem of one of claims 8 through 10, wherein at least one

said host-side IO device interconnect port is Serial ATA operating in target mode.

45. (withdrawn) An external JBOD emulation controller for emulating IO operations in response to IO requests from a host entity, comprising:

a central processing circuitry for performing IO operations in response to said IO requests of said host entity;

at least one IO device interconnect controller coupled to said central processing circuitry;

at least one host-side IO device interconnect port provided in a said at least one IO device interconnect controller for coupling to said host entity; and

at least one device-side IO device interconnect port provided in a said at least one IO device interconnect controller for coupling to a set of at least one physical storage device for performing point-to-point serial signal transmission therebetween, wherein

said JBOD emulation controller is capable of being configured to define at least one logical media unit (LMU) comprising sections of at least one of said PSDs and being brought on line or taken off line while said JBOD emulation controller is on line.

46. (withdrawn) The external JBOD emulation controller of claim 45 wherein a said device-side IO device interconnect port is a Serial ATA IO device interconnect port, each for connecting to a said physical storage devices through a Serial ATA IO device interconnect.

47. (withdrawn) The external JBOD emulation controller of claim 45 wherein a said device-side IO device interconnect port is a Serial-Attached SCSI (SAS) IO device interconnect port, each for connecting to a said physical storage devices through an SAS IO device interconnect.

48. (withdrawn) The external JBOD emulation controller of one of claims 45 through 47 wherein further comprises:

a PCI/PCI-X/PCI Express interface for connecting to the central processing circuit; and

a Dec/Mux arbiter coupled to the PCI/PCI-X/PCI Express interface and a plurality of said device-side IO device interconnect ports for selectively communicating the PCI/PCI-X/PCI Express interface with one of said device-side IO device interconnect ports.

49. (withdrawn) The external JBOD emulation controller of one of claims 45 through 47 wherein a said LMU is capable of being brought on line while said JBOD emulation controller is on line.

50. (withdrawn) The external JBOD emulation controller of one of claims 45 through 47 wherein a said LMU is capable of being taken off line while said JBOD emulation controller is on line.

51. (withdrawn) The external JBOD emulation controller of one of claims 45 through 47 wherein a said at least one LMU comprises sections of a plurality of the physical storage devices.

52. (withdrawn) The external JBOD emulation controller of one of claims 45 through 47, further comprising determining mechanism for automatically determining when a PSD has been removed or when one has been inserted.

53. (withdrawn) The external JBOD emulation controller of one of claims 45 through 47, further comprising scanning-in mechanism to automatically scan in PSDs on detection of insertion of the PSD.

54. (withdrawn) The external JBOD emulation controller of claim 51, further comprising auto-on-lining mechanism for automatically bringing on line a said LMU which was previously off-line on detection of insertion of a said PSD associated with said LMU.

55. (withdrawn) The external JBOD emulation controller of claim 51, further comprising auto-off-lining mechanism for automatically taking off line a said LMU which was previously on-line on detection of off-lining of all PSDs associated with said LMU.

56. (withdrawn) The external JBOD emulation controller of one of claims 45 through 47, further comprising informing mechanism for informing the host entity when the mapping of said LMUs to host-side interconnect LUNs has changed.

57. (withdrawn) The external JBOD emulation controller of claim 56, wherein said at least one host-side IO device interconnect is a Fibre operating in Arbitrated Loop mode and said external JBOD emulation controller issues a LIP when a new target ID is introduced onto the Fibre loop so as to inform other devices on the loop that the loop device map has changed.

58. (withdrawn) The external JBOD emulation controller of claim 56, wherein said at least one host-side IO device interconnect is a Fibre operating in Arbitrated Loop mode and said external JBOD emulation controller issues a LIP when a target ID is removed from the Fibre loop so as to inform other devices on the loop that the loop device map has changed.

59. (withdrawn) The external JBOD emulation controller of one of claims 45 through 47, wherein standard SCSI command set is used as a primary command interface with the host entity over the host-side IO device interconnects.

60. (withdrawn) The external JBOD emulation controller of one of claims 45 through 47, wherein said external JBOD emulation controller is capable of posting a CHECK CONDITION status to the host with sense data to inform the host when the mapping of LMUs to host-side interconnect LUNs has changed.

61. (withdrawn) The external JBOD emulation controller of one of claims 45 through 47, further comprising unique ID determination mechanism to uniquely identify said PSDs.

62. (withdrawn) The external JBOD emulation controller of claim 61, wherein information used to uniquely identify each of said PSDs is stored on the PSD.

63. (withdrawn) The external JBOD emulation controller of one of claims 45 through 47, wherein LMU identification and configuration information is stored on the member PSDs that compose the LMU.

64. (withdrawn) The external JBOD emulation controller of claim 63, wherein LMU identification information presented to the host entity is generated from said LMU identification information stored on the member PSDs that compose the LMU.

65. (withdrawn) The external JBOD emulation controller of one of claims 45 through 47, wherein LMU identification information presented to the host entity is generated from information stored in a non-volatile memory in the JBOD emulation controller.

66. (withdrawn) The external JBOD emulation controller of one of claims 45 through 47, wherein LMU identification information presented to the host entity is generated as follows: from information stored in a non-volatile memory in the JBOD subsystem prior to being able to obtain LMU identification information off of the member PSDs

and from LMU identification information stored on the member PSDs that compose the LMU after the member PSDs become accessible.

67. (withdrawn) The external JBOD emulation controller of one of claims 45 through 47, wherein at least one said host-side IO device interconnect port is Fibre Channel supporting point-to-point connectivity in target mode.

68. (withdrawn) The external JBOD emulation controller of one of claims 45 through 47, wherein at least one said host-side IO device interconnect port is Fibre Channel supporting public loop connectivity in target mode.

69. (withdrawn) The external JBOD emulation controller of one of claims 45 through 47, wherein at least one said host-side IO device interconnect port is Fibre Channel supporting private loop connectivity in target mode.

70. (withdrawn) The external JBOD emulation controller of one of claims 45 through 47, wherein at least one said host-side IO device interconnect port is parallel SCSI operating in target mode.

71. (withdrawn) The external JBOD emulation controller of one of claims 45 through 47, wherein at least one said host-side IO device interconnect port is ethernet supporting the iSCSI protocol operating in target mode.

72. (withdrawn) The external JBOD emulation controller of one of claims 45 through 47, wherein at least one said host-side IO device interconnect port is Serial-Attached SCSI (SAS) operating in target mode.

73. (withdrawn) The external JBOD emulation controller of one of claims 45 through 47,

wherein at least one said host-side IO device interconnect port is Serial ATA operating in target mode.

74. (withdrawn) The external JBOD emulation controller of one of claims 45 through 47, further comprising ID generation mechanism to automatically generate the LMU identification information presented to the host entity when a need arises.

75. (withdrawn) The external JBOD emulation controller of one of claims 45 through 47, further comprising an enclosure management services (EMS) mechanism.

76. (withdrawn) The external JBOD emulation controller of claim 75, wherein said EMS mechanism is of a direct-connect EMS configuration.

77. (withdrawn) The external JBOD emulation controller of claim 75, wherein said EMS mechanism is of a device-forward EMS configuration.

78. (withdrawn) The external JBOD emulation controller of claim 75, wherein said EMS mechanism implements both direct-connect and device-forward EMS configurations.

79. (withdrawn) The external JBOD emulation controller of claim 75, wherein said JBOD emulation controller is configured to support SES enclosure management services protocol.

80. (withdrawn) The external JBOD emulation controller of claim 75, wherein said JBOD emulation controller is configured to support SAF-TE enclosure management services protocol.

81. (withdrawn) The external JBOD emulation controller of one of claims 45 through 47,

further comprising notifying mechanism for having the host entity duly informed of a change in LMU mapping when LMU identification information presented to the host entity changes due to a discrepancy between information stored on the JBOD emulation controller and the actual identification information read off of the PSDs.

82. (withdrawn) The external JBOD emulation controller of one of claims 45 through 47 wherein said LMU are presented redundantly to the host entity on more than one host-side IO device interconnect port.

83. (original) A method for performing JBOD emulation in a computer system having at least one external JBOD emulation controller and a set of at least one physical storage device connected to the JBOD emulation controller, the method comprising:
defining at least one logical media unit (LMU) comprising sections of said set of at least one of the physical storage device by the JBOD emulation controller;
receiving and parsing IO requests from a host entity by the JBOD emulation controller to perform an IO operation to access the LMU by accessing said set of at least one of the physical storage device through at least one device-side IO device interconnect port in point-to-point serial signal transmission; and,
while the JBOD emulation controller is on line, bringing on line a said at least one logical media unit which is not on line or taking off line a said at least one logical media unit which is on line.

84. (original) The method of claim 83 wherein the device-side IO device interconnect port is a Serial ATA IO device interconnect port.

85. (original) The method of claim 83 wherein the device-side IO device interconnect port is a Serial-Attached SCSI (SAS) IO device interconnect port.

86. (original) The method of one of claims 83 through 85 further comprising: while the JBOD emulation controller is on line, bringing on line a said at least one LMU which is not on line.

87. (original) The method of one of claims 83 through 85 further comprising: while the JBOD emulation controller is on line, taking off line a said at least one LMU which is on line.

88. (original) The method of one of claims 83 through 85 wherein said at least one LMU comprises sections of a plurality of the physical storage devices.

89. (original) The method of claim 88, further comprising automatically bringing on line a said LMU which was previously off-line on detection of insertion of a said PSD associated with said LMU.

90. (original) The method of claim 88, further comprising automatically taking off line a said LMU which was previously on-line on detection of off-lining of all PSDs associated with said LMU.

91. (original) The method of claim 87, wherein said at least one host-side IO device interconnect port supports one of the following: Fibre Channel supporting point-to-point connectivity in target mode, Fibre Channel supporting public loop connectivity in target mode, Fibre Channel supporting private loop connectivity in target mode, parallel SCSI operating in target mode, ethernet supporting the iSCSI protocol operating in target mode, Serial-Attached SCSI (SAS) operating in target mode, and Serial ATA operating in target mode.

92. (original) A computer-readable storage medium having a computer program code

stored therein that is capable of causing a computer system having an external JBOD emulation controller and a set of at least one physical storage device connected to the JBOD emulation controller to perform the steps of:

defining at least one logical medium unit comprising sections of at least one of the physical storage devices by the JBOD emulation controller; and

receiving and parsing IO requests from a host entity by the JBOD emulation controller to perform an IO operation to access the logical media unit (LMU) by accessing said set of at least one physical storage device through at least one device-side IO device interconnect in point-to-point serial signal transmission, wherein

said JBOD emulation controller is capable of performing one of the followings while being on line: bringing on line a said at least one LMU which is not on line and taking off line a said at least one LMU which is on line.

93. (original) The computer-readable storage medium of claim 92 wherein the device-side IO device interconnect is a Serial ATA IO device interconnect.

94. (original) The computer-readable storage medium of claim 92 wherein the device-side IO device interconnect is a Serial-Attached SCSI (SAS) IO device interconnect.